A METHOD AND APPARATUS FOR DIRECTORY-BASED COHERENCE WITH DISTRIBUTED DIRECTORY MANAGEMENT

ABSTRACT

The present invention provides for a type of parallel processing architecture in which a plurality of processors has access to a shared memory hierarchy level. A memory hierarchy level has a coherence directory and associated directory data with a plurality of cachelines each associated with different data. Prefetch caches are interconnected to processor memory and a plurality of processor elements, each element interconnected to different buffers. Cache lines are requested from memory, and the requests, responses, and detections therein are available for particular access modes, therein providing additional coherence of the data. Processing of said directory data is performed by processing elements. In one embodiment, the system comprises an integrated prefetch cache.